**ECE 429 Lab 9**

**Standard Cell Based ASIC Design Flow**

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**Introduction**

The objective of this lab is to become familiar with the concept of a standard cell-based ASIC design flow. This is accomplished using the tutorial provided in the lab.

**Theory**

The standard cell-based ASIC design flow automatically synthesizes a chip layout. This is accomplished using a register-transfer-level (RTL) description of the desired functionality. This design flow consists of two steps: logic synthesis and physical design.

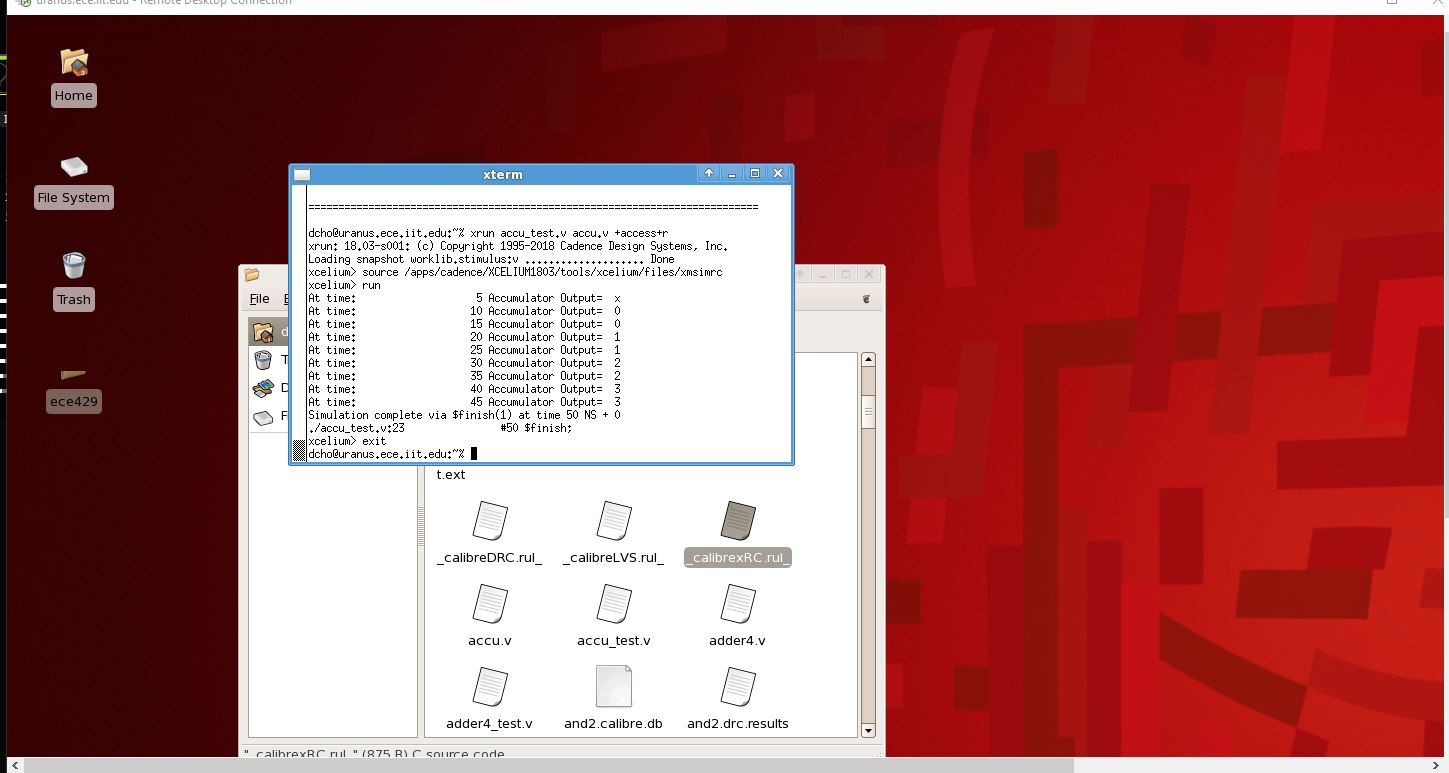
Logic synthesis transforms RTL descriptions into a netlist consisting of standard cells that will be implemented on a chip. After synthesis, the logic tool performs generic logic optimizations to optimize the design. Then it creates a netlist consisting of standard cells that have the same Boolean functionality as the one generated by generic logic optimizations.

Physical design creates a physical implementation of the netlist consisting of standard cells. Cadence Encounter Digital Implementation System will be used for physical design.

**Implementation**

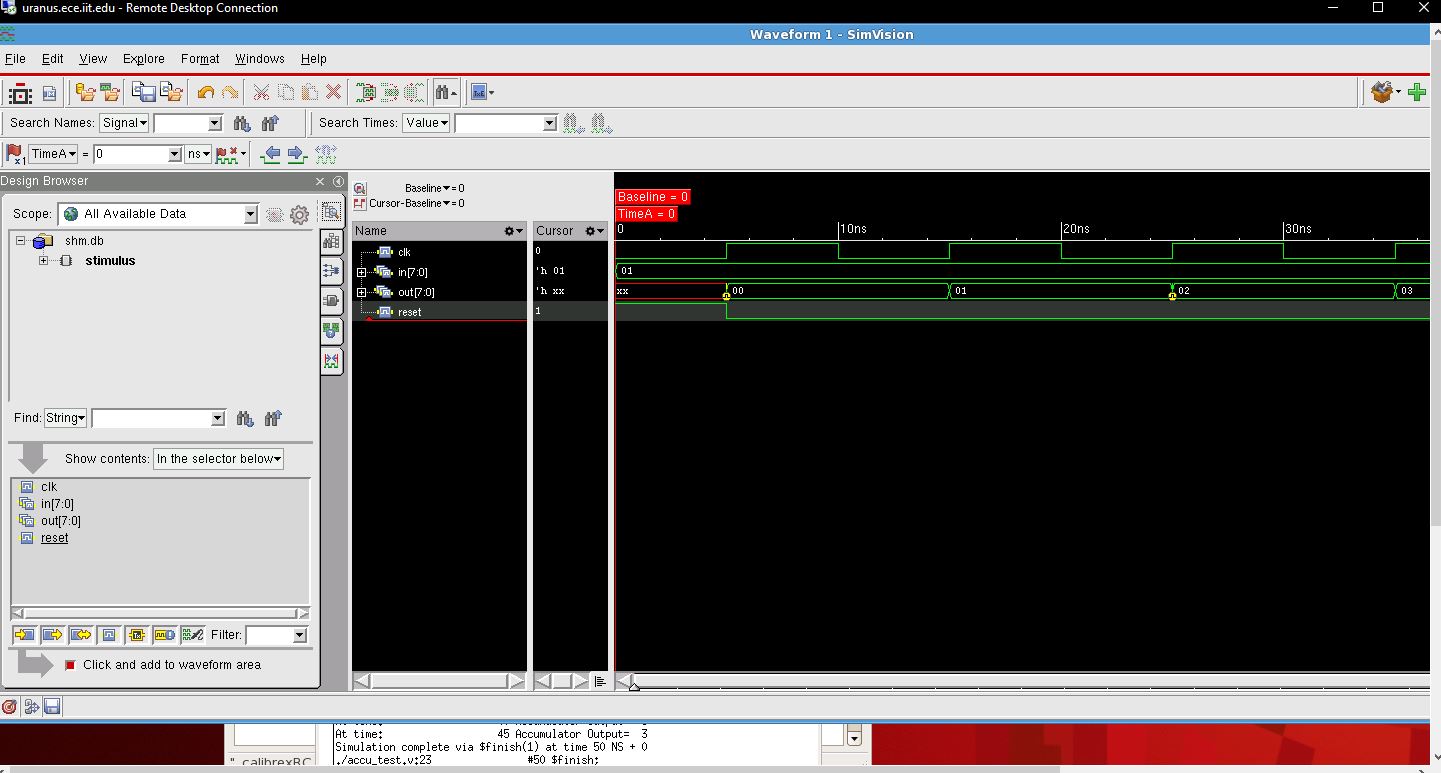
Using the tutorial, a testbench was ran for the Verilog codes of accu.v and accu\_test.v, both of which were provided in the tutorial.

**Figure 1: Verilog testbench**

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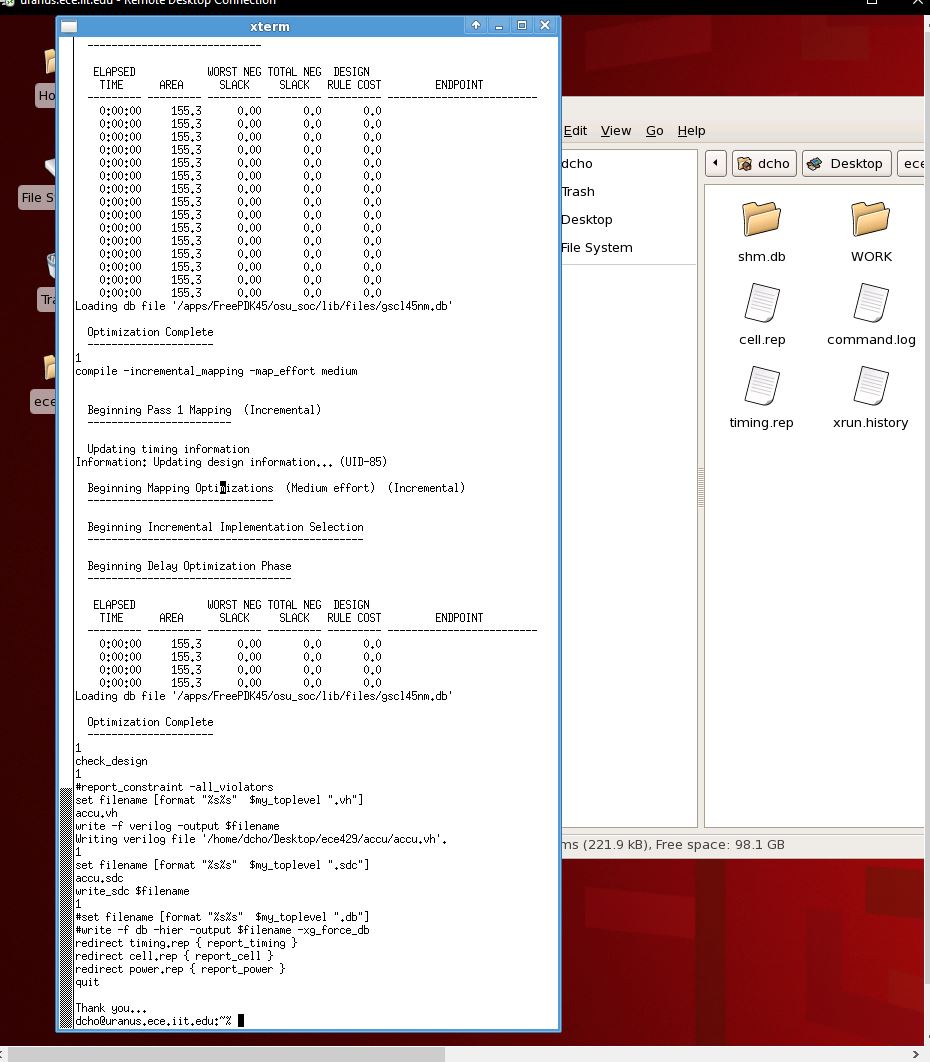
A graphical representation of the results was then observed using Simvision.

**Figure 2: Simvision**

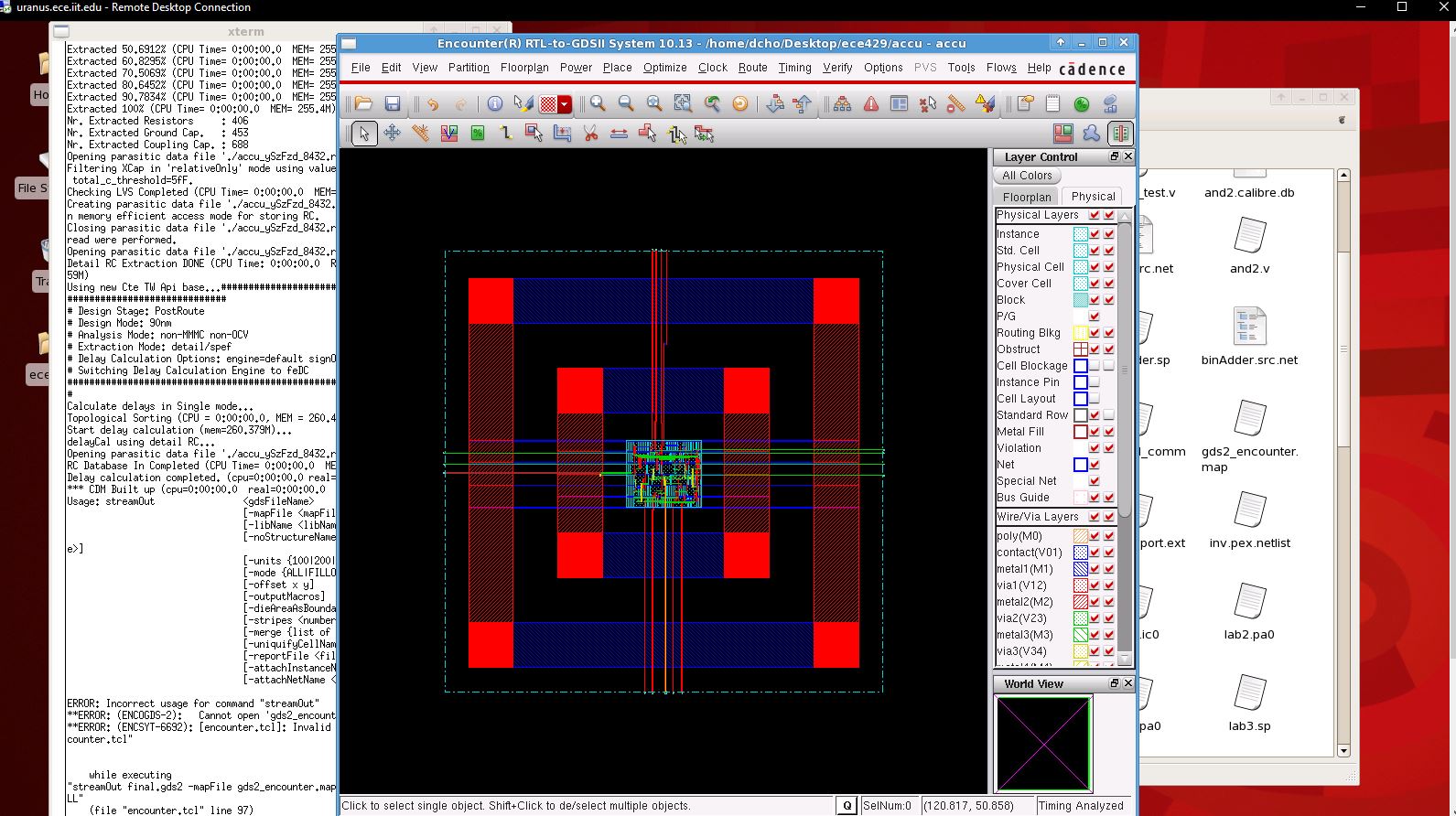
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Logic synthesis was then done using the Design Compiler.

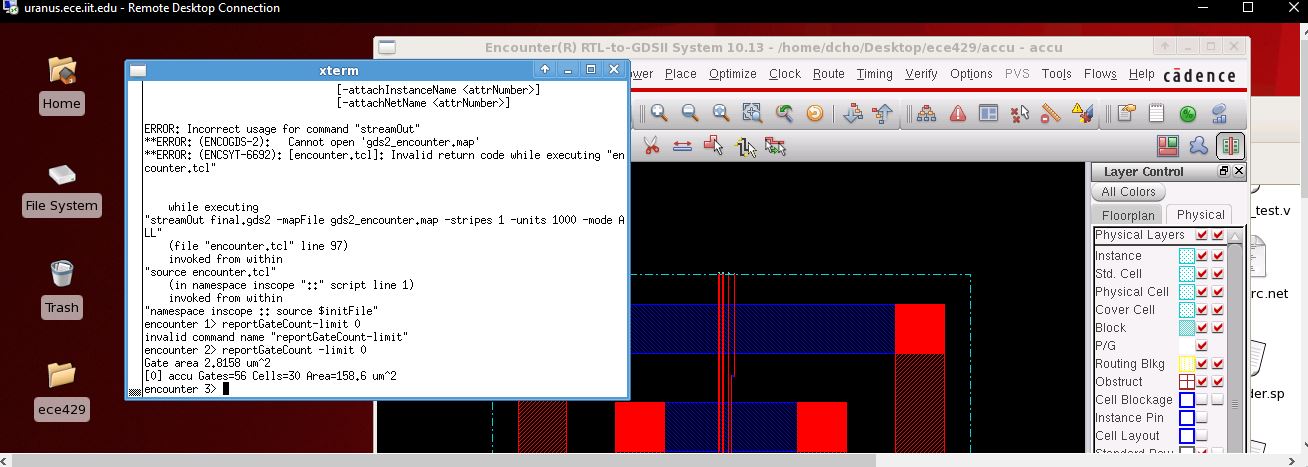
**Figure 3: Logic Synthesis**

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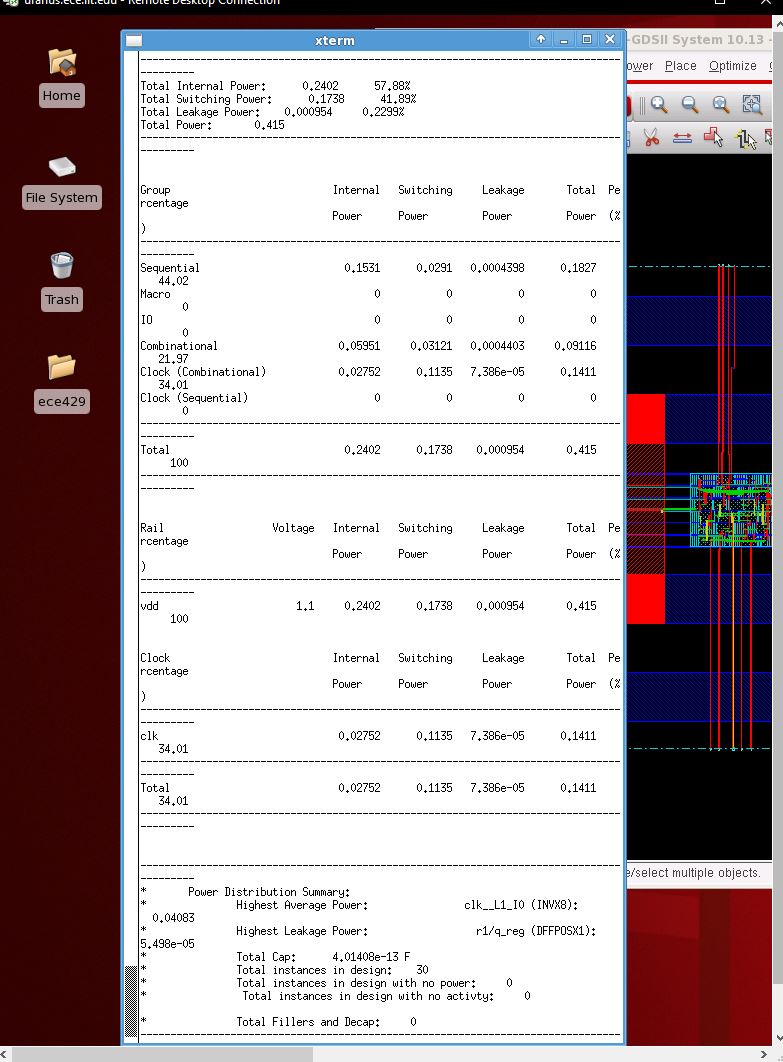
Encounter was then used to automate placement and route task. Encounter also allowed an area report in addition to a power report.

**Figure 4: Place and Route**

**Figure 5: Area Report**

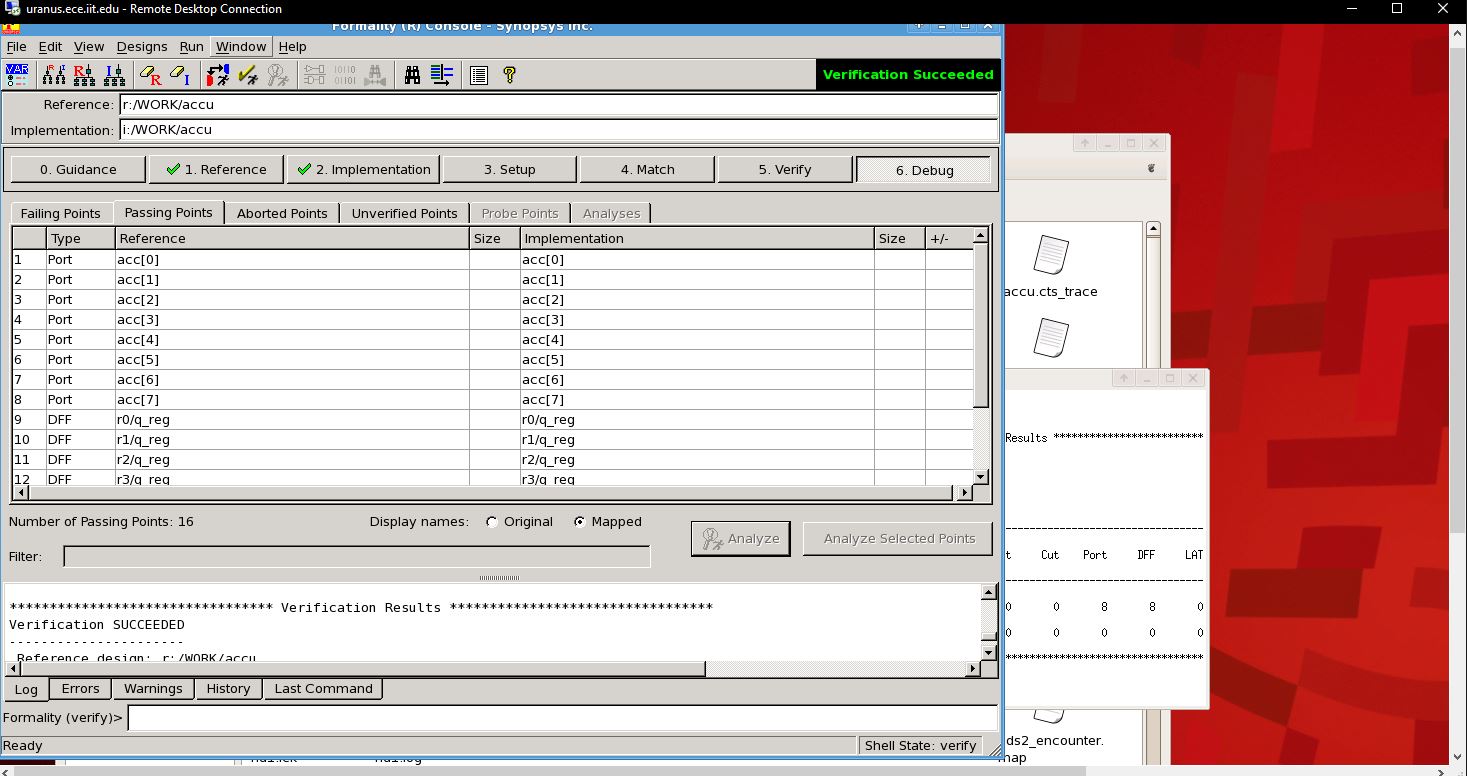
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**Figure 6: Power Report**

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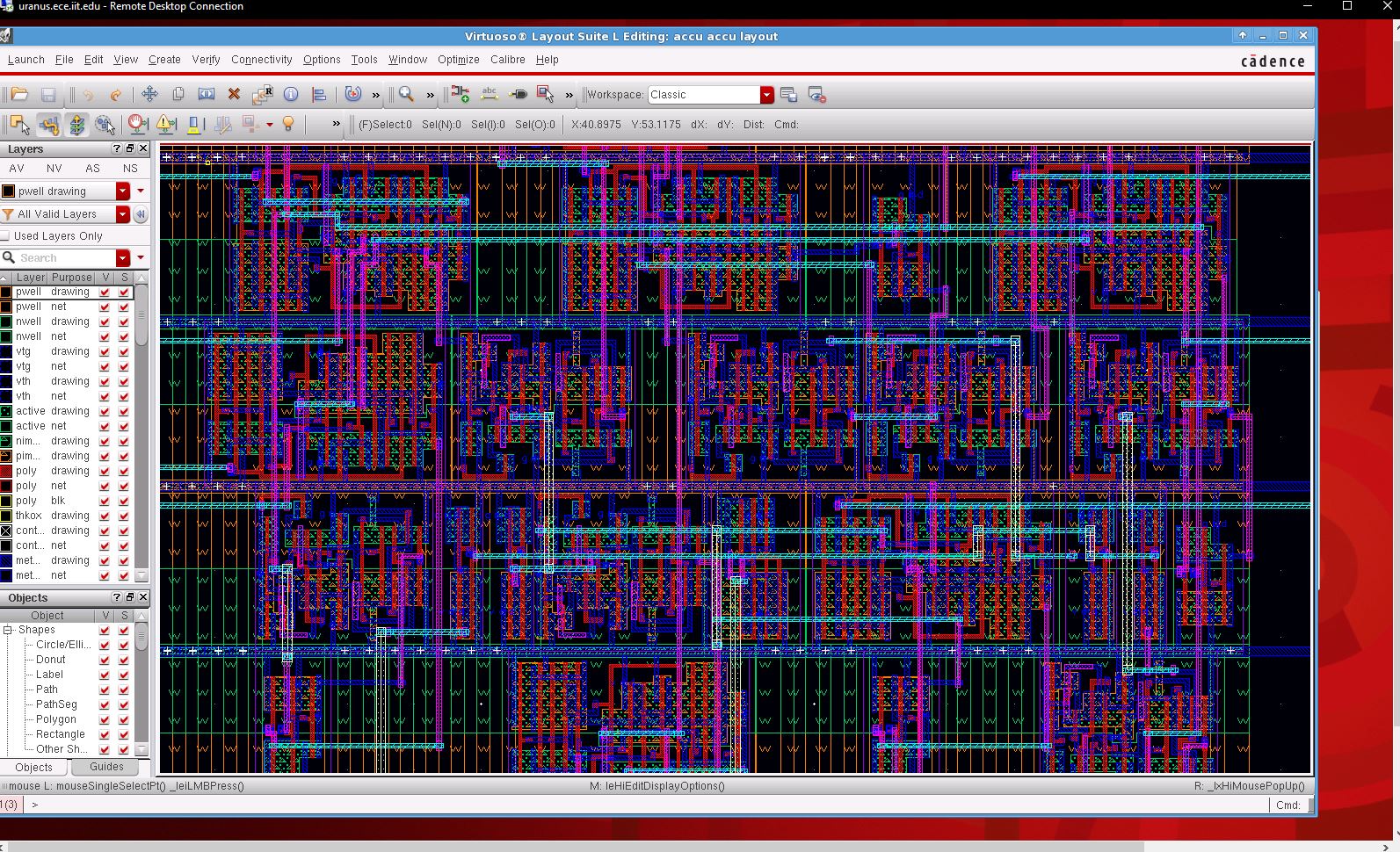
Formality was then used to Equivalence check the final.v that was created from Encounter.

**Figure 7: Formality ESP**

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The final print was then observed using Virtuoso.

**Figure 8: Final Layout**

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**Deliverable Questions**

1. A standard cell is a group of transistors . They provide Boolean logic functions. Altogether, they work to produce complex circuits.
2. *accu.v* is the Verilog file created by me*. accu.vh* was generated by the logic synthesis. *final.v* is the Verilog file created from Encounter.
3. The area is smaller after place & route because the design is then optimized.
4. The time becomes faster after place & route because the design is then optimized.
5. *final.gds2* contains the placement of the cells and the metal interconnects. Virtuoso is required for the other layout details.

**Conclusion**

In conclusion, this was a successful lab. Although there was some trouble getting the benchmark to work at the beginning, the kinks were worked out and it was smooth sailing. The tutorial was easy to follow, and the results were as expected.